中 華 民 國 專 利 公 報 〔19〕〔12〕

〔11〕公告編號：162395

〔44〕中華民國80年（1991）07月01日

〔51〕Int.Cl.5：G11C7/03

發 明 全 3 頁

911 6270

〔54〕名 稱：含有一並列與串列輸入與輸出之積體記憶電路

〔21〕申 請 案 號：78110052 〔22〕申請日期：中華民國78年（1989）12月27日

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[57]申請專利範圍：

1.一種積體記憶電路，包括一矩陣，其中每一欄均包括其本身之感測放大電路，用以在各感測放大電路輸出上形成可呈現於外之輸出信號，該電路之特點爲每一感測放大電路均有閂鎖功能，且置有選擇裝置用以選擇若干個感測放大電路，每個均構成各對感測放大電路之一部分，同時亦置有轉移裝置，直接以相關欄對中另一感測放大電路之資訊取代該相關對中一個感測放大電路之資訊，而此一感測放大電路之資訊即被銷毀。

2.根據申請專利範圍第1項之積體記憶電路，其中在一對中之兩個感測放大電路直接相鄰，其中一個感測放大電路之增益高於或等於在控制信號影響下另一感測放大電路之增益。

3.根據申請專利範圍第2項之積體記憶電路，其中各感測放大電路均有組合之輸入與輸出。

4.根據申請專利範圍第3項之積體記憶電路，其中一欄中每一感測放大電路之輸入均經由適於接收兩個不同控制信號之個別可

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交換疊接元件，連接至相關欄中之位元線。

5.根據申請專利範圍第3項之積體記憶電路，其中每一可交換串列元件均包括一n型電晶體。

6.根據申請專利範圍第4項之積體記憶電路，其中每一可交換疊接元件均包括並聯之P型電晶體與n型電晶體。

7.根據申請專利範圍第5項之積體記憶電路，其中從一奇數欄至一欄號增加之偶數欄各n型電晶體之控制電極均適於接收第一控制信號及自一偶數欄至一欄號增加之奇數欄之第二控制信號。

8.根據申請專利範圍第6項之積體記憶電路，其中每一可交換疊接元件中P型電晶體之控制電極均適於接收一讀取信號，奇數與偶數欄中每一可交換疊接元件內n型電晶體之控制電極均分別適於接收第一與第二書寫信號。

9.根據申請專利範圍第7項之積體記憶電路，其中各奇數與偶數欄中之感測放大電路均適於分別接收第一與第二控制信號或第

第 9111.6270 號
初審 ~~再審~~ (新穎) 引證附件

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類 別	G11C /03

(以上各欄由本局填註)

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發明/新型 專利說明書

一、發明/創作 名稱	中 文	含有一並列與串列輸入與輸出之積體記憶電路
	英 文	INTEGRATED MEMORY CIRCUIT COMPRISING A PARALLEL AND SERIAL INPUT AND OUTPUT
二、發明/創作 人	姓 名	1.[illegible] JUDOCUS ADRIANUS MARIA LAMMERTS 2.[illegible] RICHARD CHARLES FOSS 3.[illegible] ROELOF HERMAN WILLEM SALTERS
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	代表人 姓 名	[illegible] IWAN MILLAR LERNER

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五、發明說明（1）

本發明係關於一種積體記憶電路，包括一矩陣，其中之每欄包括其本身之感測放大器電路用以形成各感測放大器電路輸出上可呈現於外之輸出信號。

美國第 3,930,239 號專利規格中曾揭露此種電路。

該專利規格中說明一種積體記憶電路，其中附加轉換記發器之使用能使對記憶體中之資料作快速之串列寫讀。此種記憶體之缺點爲該額外之轉換記發器使得晶片須有較大之表面面積。

本發明目的之一即在提供一種積體記憶電路，其中之資料可按照選擇以串列或並列方式快速寫入或讀出記憶體，但却不需要額外之轉換記發器，使積體記憶電路之晶片表面面積仍能保持很小。

爲達此目的，本發明積體記憶電路之特點爲每一感測放大器電路均有閂鎖功能，且置有選擇裝置用以選擇若干感測放大器電路，每個均構成各對感測放大電路之一部分，同時亦置有轉換裝置用以在相關對中以另一感測放大電路之資訊直接取代一個感測放大電路之資訊而將此一感測放大電路中之資訊予以銷毀。該轉換裝置能使選出記憶格之資訊直接加至或移自鄰接之欄。資訊可自一欄運輸至另一欄，使得資訊可出現於任何所需之欄。再者，資訊可按照選擇以並列方式寫入記憶體或自其中讀出。積體電路之記憶體可僅經由連接至晶片之一個輸入接頭藉外供資料加以序列程式化。因此，例如積體電路晶片上之微處理器即能以並列方式自記憶體讀取資料（例如，可能含有串列位元

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五、發明說明（2）

之指令）。

本發明之積體記憶電路提供一項優點，即所需之感測放大電路及額外之交換元件可用做轉換記發器而使感測放大器有雙重功能。額外之交換裝置元件較之前述轉換記發器所需之晶片表面面積爲小而使整個積體記憶電路之面積較小。

本發明積體記憶電路一項實例之特點爲一對中之兩個感測放大電路直接相鄰，在一控制信號影響下，其中一個感測放大電路之增益較另外一個者爲高或相等。自n欄轉移至n＋1欄或反之自n＋1欄至n欄之資訊方向全視相關欄中感測放大電路之各增益而定。具有較高增益欄中之資訊轉移至具有較低增益之欄中，因而界定資訊轉移之方向。因一對中兩個感測放大電路直接相鄰，兩電路間連接所需之晶片表面面積甚小。

本發明積體記憶電路一項較佳實例之特點爲感測放大電路包括組合之輸入與輸出。因此可有一標準之正反器結構，在一欄中之正反器爲主，而相鄰欄中者爲附。不使用額外交換裝置即能以串列方式將資訊寫入記憶格中及自其中讀出。

本發明亦關於一種積體電路，包括一處理器、一資料匯流排及一記憶電路，處理器經由資料匯流排連接至記憶電路之輸入與輸出。因此，處理器之任何程式作業（假如字寬爲32位元之指令）僅須一個積體電路之連接桿（並列程式者須有32個連接桿）而使得積體電路體積更小。

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五、發明說明（3）

現藉附圖對本發明詳加說明：

圖 1 爲本發明之記憶電路。

圖 2 爲圖 1 記憶電路較佳實例一部份之詳細顯示。

圖 3 爲圖 1 記憶電路較佳實例另一部分之詳細顯示。

圖 1 所示爲本發明記憶電路之一部分，該記憶電路包括：

一一記憶格矩陣 $M_{i,j}$，排成 m 排與 n 欄，m 與 n 分別爲排與欄之數目，在 j 欄中之記憶格 $M_{i,j}$（此處 j 爲偶數）經由兩個位元線（BIT_j 及 $\overline{BIT}_j$）互接，i 排中之全部記憶格接收一排選擇信號 WL_i。

一每一 j 欄中有一感測放大電路 A_j，經由放大控制線SA接收一共用控制信號，奇數與偶數欄中之感測放大電路亦分別經由第一選擇線 FODD 與第二選擇線 FEVEN接收控制信號。

一每一 j 欄分別有疊接元件 SL_j 及 SR_j 將 j 欄中分別連接至資料線 D_j 與 $\overline{D}_j$ 之感測放大電路 A_j 之輸入與輸出耦合至位元線 BIT_j 及 $\overline{BIT}_j$，j 欄中接連至共同讀取控制線（奇數欄中之 1，…，j－1，j＋1…及偶數欄中 2，…，j，j＋2…等）之元件 SL_j 及 SR_j 亦分別連接至第一書寫線 WRODD 及第二書寫線 WREVEN。

一交換元件 L 與 R 可連接二相鄰之 j 與 j＋1 欄、資料線 D_j 至 D_{j+1} 及 $\overline{D}_j$ 至 $\overline{D}_{j+1}$，L_j 與 R_j 元件將 j 欄連接至相接之 j＋1 欄（藉著對第二選擇線 FEVEN 供以控制信號），元件 L_{j-1} 及 R_{j-1} 藉第一選擇線 FODD 上之控制信號將奇數欄 j－1 連接至偶數欄 j。

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五、發明說明（4）

後文中必須爲邏輯低或邏輯高之信號將分別簡稱爲低或高。

圖1所示記憶電路一部分之作業將由將資訊寫入或讀出記憶格$M_{i,j}$加以說明。

爲求自一排記憶格$M_{i,j}$讀出資訊，下述之控制信號具有下述之邏輯位準：

字線WL_i上之控制信號變爲「高」而使i排中之全部記憶格$M_{i,j}$被選，結果在全部位元線BIT及$\overline{BIT}$上均出現邏輯信號。隨後讀取控制線$\overline{READ}$上之控制信號即變爲「低」而使1，2，…，j，…，n各欄中之疊接元件SL_{j-1}，SR_{j-1}，SR_j，SL_{j+1}，SR_{j+1}等分別將位元線BIT_j及$\overline{BIT}_j$連接至感測放大電路A_j及資料線D_j與$\overline{D}_j$。當隨後之「高」控制信號出現於放大控制線SA上時，每一感測放大電路A_j即擷取位元線BIT_j及$\overline{BIT}_j$及資料線D_j與$\overline{D}_j$上出現之資訊而將此等信號放大暫時保留起來。

每一感測放大電路A_j及資料線D_j與$\overline{D}_j$輸出上之資訊隨後可被並列轉移至其他在圖中未示出之電路，例如至晶片上微處理器。

但每一感測放大電路A輸出上之資訊在讀取記憶格$M_{i,j}$之i排後，亦可串列而非並列轉移至積體記憶電路中之電路（未示出），例如至一微處理器。本發明資訊之串列呈現方式如下：j欄中之資訊線D_j與$\overline{D}_j$經由交換元件L_j與R_j連接至直接相鄰之j＋1欄中之資料線D_{j+1}與$\overline{D}_{j+1}$。圖中顯示交換元件L_{j-1}與R_{j-1}分別將j－1欄中之資

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五、發明說明（5）

料線 D_{j-1} 與 $\overline{D}_{j-1}$ 連接至 j 欄中之資料線 D_j 與 $\overline{D}_j$，交換元件 L_j 與 R_j 分別將 j 欄中之資料線 D_j 與 $\overline{D}_j$ 連接至 j + 1 欄中之資料線 D_{j+1} 與 $\overline{D}_{j+1}$。當交換元件 L_{j-1} 及 R_{j-1} 以及 L_{j+1} 與 R_{j+1} 等被線 FODD 上之「高」選擇信號所選，而交換元件 L_{j+2} 與 R_{j+2}（未示出）因爲線FEVEN上之信號爲「低」而被選擇時，資訊即可由 j－1 欄流至 j 欄或反之由 j 欄流至 j－1 欄。同樣地，資訊可由 j＋1 欄流至 j＋2 欄或反之由 j＋2 欄流至 j＋1 欄。從 j 欄到 j＋1 欄或反之從 j 欄到 j－1 欄之資訊轉移方向視相關 j－1、j、j＋1、j＋2 欄中感測放大電路之增益而定。放大控制線SA上之控制信號在串列轉移時爲「高」，使得自相鄰感測電路接收資訊之感測放大電路取得此一資訊並將之保留。資訊之轉移係由具有較高增益感測放大電路之欄至具有較低增益感測放大電路之欄，後者欄中之資訊會因原存資訊被來自增益較高欄中之新資訊取代而消失。

感測放大電路增益間所需之鑑別亦係藉選擇線 FODD 及 FEVEN 上之信號而完成。在選擇信號出現於線 FODD 上而線 FEVEN 上並無選擇信號時，感測放大電路 A_{j-1} 之增益高於感測放大電路 A 之增益。因圖 1 中之感測放大電路 A_{j-1}、A_{j+1} 等及交換元件 L_{j-1} 與 R_{j-1} 及 L_{j+1} 與 R_{j+1} 等均係經由線 FODD 接收控制信號，而感測放大電路 A_j、A_{j+2} 等及交換元件 L_j 與 R_j 及 L_{j+2} 與 R_{j+2} 等均經由線 FEVEN 接收控制信號，資訊則從 j 欄移轉至 $_{j+1}$ 欄。當感

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五、發明說明（6）

測放大電路 A_j 與 A_{j-1} 之驅動倒反（分別以經由線 FEVEN 與 FODD 之驅動取代經由線 FODD 與 FEVEN 之驅動）而交換元件 L_j 與 R_j 保持不變，或交換元件 L_j 、R_j 以及 L_{j-1} 、R_{j-1} 之驅動倒反而感測放大電路 A_j 之驅動保持不變時，後者之資訊轉移方向亦倒反而資訊是由 j 欄轉移至 j－1 欄。但若增加簡單之雙工電路及對之加上一控制信號會使資訊之轉移如所需地從 j 欄到 j＋1 欄或從 j 欄到 j－1 欄。附加之控制信號使雙工電路將感測放大電路 A_j 、A_{j+1} 等連接至線 FODD 或線 FEVEN ，而將感測放大電路 A_{j-1} 與 A_{j+1} 連至線 FEVEN 或線 FODD 。在前者情形下，資訊由右向左轉移，後者之情形則由左至右。爲簡明計，後文中線上之信號將以相關線之符號表示之。

欲將資訊串列轉移至積體記憶電路內之電路（未示出），控制信號 FODD 與 FEVEN 在時間觀點上之位準如下：控制信號SA爲「高」，控制信號 FODD 爲「高」而控制信號 FEVEN 爲「低」，使得資訊轉移爲自 j－1 欄至 j 欄及自 j＋1 欄至 j＋2 欄等。因此，控制信號 FODD 變爲「低」而控制信號 FEVEN 變爲「高」，使得資訊轉移係從 j 欄至 j＋1 欄及從 j＋2 欄至 j＋3 欄等。控制信號 FODD 再變爲「高」而控制信號 FEVEN 再變爲「低」，使得資料轉移發生於下一欄中等。控制信號 FODD 與 FEVEN 交互變爲「高」與「低」，直至全部所需資訊轉移至積體記憶電路之電路中（未示出）爲止。上述之控制信號 FODD 與FEVEN 之順序確使記憶體資訊（奇數欄 j－1 、j＋1 等）經由

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五、發明說明（7）

記憶電路之最後n欄而出現於積體記憶電路之電路中（未示出）。使用上述控制信號FODD與FEVEN之順序，FODD與FEVEN之啓始值在感測放大電路A，全部組合輸入與輸出上均有記憶資訊後，分別爲「低」與「高」，資訊即由偶數欄j、j＋2等呈現至積體記憶電路中之電路（未示出）。因而記憶格$M_{i,j}$全排之串列讀取應分兩個步驟，即串列讀取奇數欄j－1、j＋1等再讀偶數欄j、j＋2等，或先讀偶數欄再讀奇數欄。

記憶格i排中資訊之書寫亦可以上述讀取之兩個方式完成，亦即並列與串列。在資料線D_j與$\overline{D}_j$上資訊之並列呈現時，資訊是在有「高」控制信號SA時被擷取及保留。因此，在出現「高」信號WRODD、WREVEN及WL_i時，資訊是被存入i排之記憶格$M_{i,j}$內。另外亦可藉耦合至資料線D_{j-1}、$\overline{D}_{j-1}$與D_j、$\overline{D}_j$及D_{j+1}與$\overline{D}_{j+1}$等而不藉感測放大電路A_{j-1}、A_j、A_{j+1}等將資訊存入記憶格$M_{i,j}$中。在本例中記憶格排中資訊之串列　寫如下：將資訊呈現至記憶電路第一欄之資料線D_1與$\overline{D}_1$上，控制信號SA爲「高」，因而控制信號FODD變爲「高」而控制信號FEVEN則保持「低」。因此，相鄰第二欄內之感測放大電路A，即擷取此一資訊，因而控制信號FEVEN變爲「高」而FODD變爲「低」，使得此一資訊被第三欄中之感測放大電路所擷取，因而新資訊呈現至第一記憶欄之資料線D_1與$\overline{D}_1$，隨後控制信號FODD變爲「高」而FEVEN變爲「低」。如此，資訊即以串列方式從j欄轉移至j＋1欄。如前文對記憶

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五、發明說明（8）

格串列讀取之說明，資訊格排中資訊之串列書寫亦必須於兩步驟內完成。第一步中寫出發生於記憶格第 i 排奇數欄內，而第二步時則發生於偶數欄內，反之亦然。使用控制信號 WRODD 與 WREVEN 驅動耦接元件 SL 與 SR，分別在第一與第二步驟中被轉移至感測放大電路之資訊可分別寫入奇數與偶數欄之記憶格內，或偶數與奇數欄內。

圖 2 爲圖 1 所示記憶電路一部分較佳實例之詳細說明，亦即交換元件 L_{i-1} 與 R_{i-1} 及 L_i 與 R_i 等以及感測放大電路 A_{i-1}、A_i、A_{i+1} 等之較佳實例。交換元件 L_{i-1} 與 R_{i-1} 及 L_i 與 R_i 等每個均包括 n 型電晶體 N5 與 N6，每一感測放大電路 A 均包括四個 n 型電晶體 N1、N2、N3、N4 及 P 型電晶體 P1 與 P2。電晶體 N1 與 N2 之源極互接且連接至電晶體 N3 與 N4 之吸極。電晶體 N1 與 P1 及 N2 與 P2 之吸極互接且分別連至電晶體 N2 與 P2 及 N1 與 P1 之閘極以及資料線 D 與 $\overline{D}$。電晶體 P1、P2 及 N3、N4 之源極分別耦合至電源供應接頭 V2、V1。電晶體 N3 及 N4（j 欄中者）之閘分別接收控制信號 SA 及 FEVEN。

圖 2 所示電路之作業如下：若爲「高」控制信號 FEVEN，「低」控制信號 FODD 及「高」控制信號 SA 時，電晶體 N3 與 N4 均打開，較大之電流流至第一電源供應接頭 V1。因此，感測放大電路 A_i 之增益超過僅被控制信號 SA 而未被控制信號 FODD 所驅動之感測放大電路 A_{i+1} 之增益，即會如前述圖 1 電路之作業，資訊係自 j 欄轉移至相鄰之

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五、發明說明（9）

j＋1欄。

圖3爲圖1所示疊接元件 SL_j 與 SR_j 及 SL_{j+1} 與 SR_{j+1} 等較佳實例之詳細說明。疊接元件 SL 與 SR 分別包括並聯之n型電晶體 N7 與 N8 及 P 型電晶體 P3 與 P4。偶數（2、4、6…）記憶欄及奇數（1、3、5…）記憶欄內電晶體 N7 與 N8 之閘分別耦合至控制信號 WREVEN 及 WRODD。每一記憶欄內疊接元件 SL 與 SR 中電晶體 P3 與 P4 之閘被控制信號 $\overline{READ}$ 所控制。

圖3所示電路之作業如下：疊接元件 SL 與 SR 之功能在圖1中已予說明，因此僅說明n型與P型電晶體之功能。若爲「低」控制信號 $\overline{READ}$ 時，記憶電路內全部疊接元件 SL 與 SR 中之電晶體 P3 與 P4 均被打開，使得每個j欄中之位元線 BIT_j 均連接至資料線 D_j，而位元線 $\overline{BIT_j}$ 則連接至資料線 $\overline{D_j}$。最好使用P型電晶體而非n型電晶體做爲電晶體 P3 與 P4，因爲當資訊被讀自記憶格 $M_{i,j}$ 時，位元線 BIT_j 與 $\overline{BIT_j}$ 上之電壓通常會大於控制壓 $\overline{READ}$ 與P型電晶體臨界壓 VTHP 之總和（若供應電壓爲5V時，此一總和大約爲1V），使得電晶體 P3 與 P4 上並無電壓損失。對電晶體 N7 與 N8 而言，最好用n型電晶體，因爲連接記憶格 $M_{i,j}$ 至位元線 BIT_j 與 $\overline{BIT_j}$（圖中未示出）之電晶體通常亦爲n型者，如此若在記憶格 $M_{i,j}$ 經由位元線 BIT_j 與 $\overline{BIT_j}$ 書寫作業時，在「低」位準上並無臨界電壓損失。

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四、中文發明摘要（發明之名稱：含有一並列與串列輸入與輸出之積體記憶電路）

一種積體記憶電路，其中之記憶格係安排成排與欄，每欄包括一單獨之感測放大器。經由附加之電晶體，記憶欄可與鄰接之記憶欄相耦合，在偶數與奇數欄中感測放大器之增益可加以調整。因此，資訊能依序自一欄轉至另一欄，使得資訊不但以並列方式且可以串列方式寫入與讀出。

英文發明摘要（發明之名稱：INTEGRATED MEMORY CIRCUIT COMPRISING A PARALLEL AND SERIAL INPUT AND OUTPUT

An integrated memory circuit in which memory cells are arranged in rows and columns, each column comprising a separate sense amplifier. Via additional transistors the memory columns can be coupled to neighbouring memory columns and the gain of the sense amplifiers in the even and the odd columns is adjustable. Consequently, information can also be serially shifted from one column to another, so that the information can be written and read not only in parallel but also serially.

附註：本案已向 荷蘭 國（地區）申請專利，申請日期：1988.8.29. 案號：8802125

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六、申請專利範圍

1. 一種積體記憶電路，包括一矩陣，其中每欄均包括其本身之感測放大電路，用以在各感測放大電路輸出上形成可呈現於外之輸出信號，該電路之特點爲每一感測放大電路均有閂鎖功能，且置有選擇裝置用以選擇若干個感測放大電路，每個均構成各對感測放大電路之一部分，同時亦置有轉移裝置，直接以相關對中另一感測放大電路之資訊取代該相關對中一個感測放大電路之資訊，而此一感測放大電路之資訊即被銷毀。

2. 根據申請專利範圍第 1 項之積體記憶電路，其中在一對中之兩個感測放大電路直接相鄰，其中一個感測放大電路之增益高於或等於在控制信號影響下另一感測放大電路之增益。

3. 根據申請專利範圍第 2 項之積體記憶電路，其中各感測放大電路均有組合之輸入與輸出。

4. 根據申請專利範圍第 3 項之積體記憶電路，其中一欄中每一感測放大電路之輸入均經由適於接收兩個不同控制信號之個別可交換疊接元件，連接至相關欄中之位元線。

5. 根據申請專利範圍第 3 項之積體記憶電路，其中每一可交換串列元件均包括一 n 型電晶體。

6. 根據申請專利範圍第 4 項之積體記憶電路，其中每一可交換疊接元件均包括並聯之 P 型電晶體與 n 型電晶體。

7. 根據申請專利範圍第 5 項之積體記憶電路，其中從一奇數欄至一欄號增加之偶數欄各 n 型電晶體之控制電極均適於接收第一控制信號及自一偶數欄至一欄號增加之奇

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六、申請專利範圍

數欄之第二控制信號。

8. 根據申請專利範圍第6項之積體記憶電路，其中每一可交換疊接元件中P型電晶體之控制電極均適於接收一讀取信號，奇數與偶數欄中每一可交換疊接元件內n型電晶體之控制電極均分別適於接收第一與第二番寫信號。

9. 根據申請專利範圍第7項之積體記憶電路，其中各奇數與偶數欄中之感測放大電路均適於分別接收第一與第二控制信號或第二與第一控制信號。

10. 根據申請專利第9項之積體記憶電路，其中之每一感測放大電路均可藉n型電晶體打開或關掉，其中與後者之n型電晶體並聯有額外之n型電晶體，其控制電極適於接收第一或第二控制信號。

11. 根據申請專利範圍第5、6、7、8或10項之積體記憶電路，其中n型電晶體可為n波道場效電晶體或雙極npn電晶體，而P型電晶體則可為P波道場效電晶體或雙極pnp電晶體。

12. 一種積體電路，包括一處理器、一資料匯流排及一記憶電路，該處理器經由資料匯流排連接至如請求專利範圍第1項記憶電路之並列輸入與輸出。

13. 根據申請專利第12項之積體電路，其中記憶電路之串列輸入／輸出係連接至積體電路之一連接墊。

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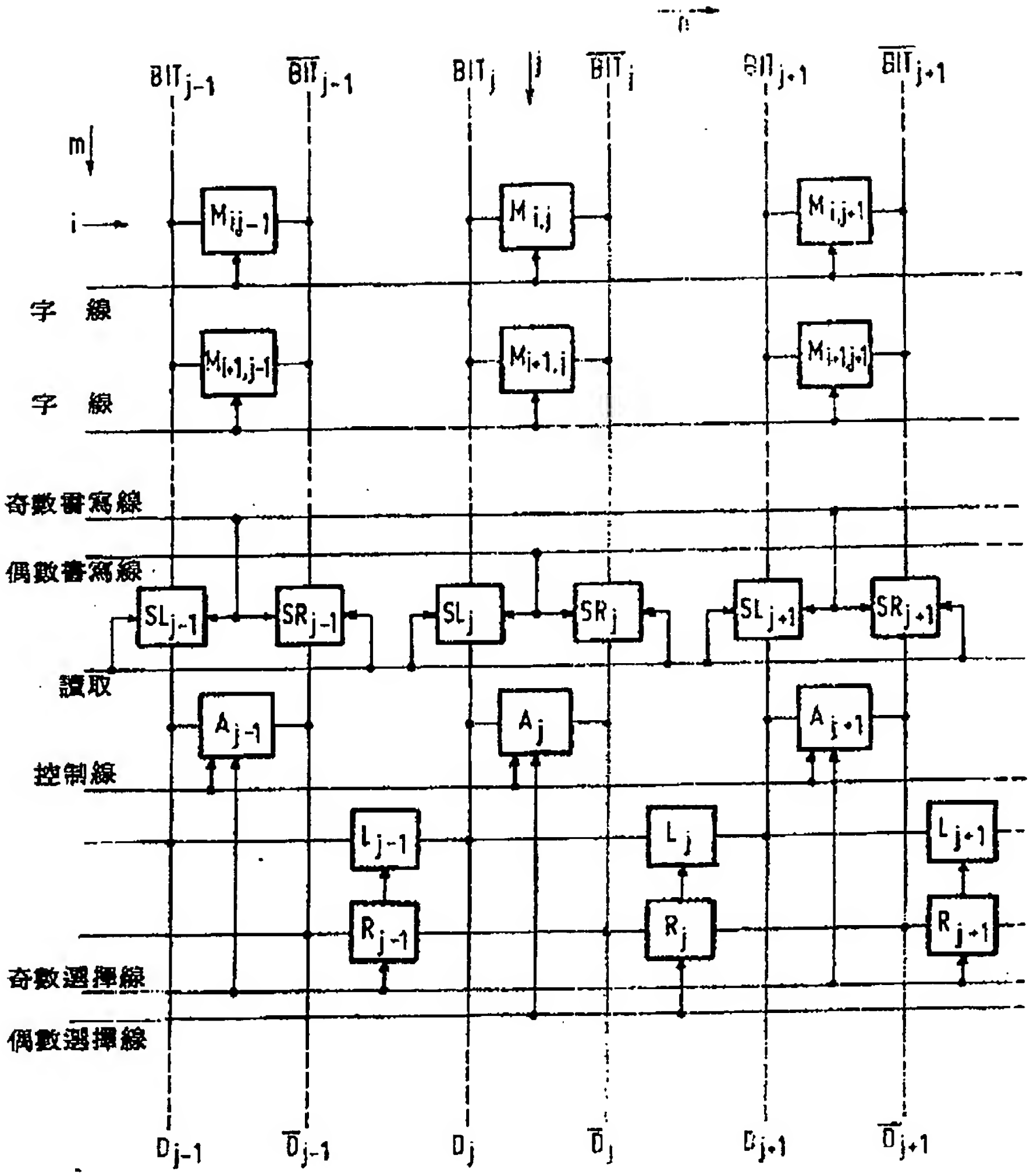

圖 1

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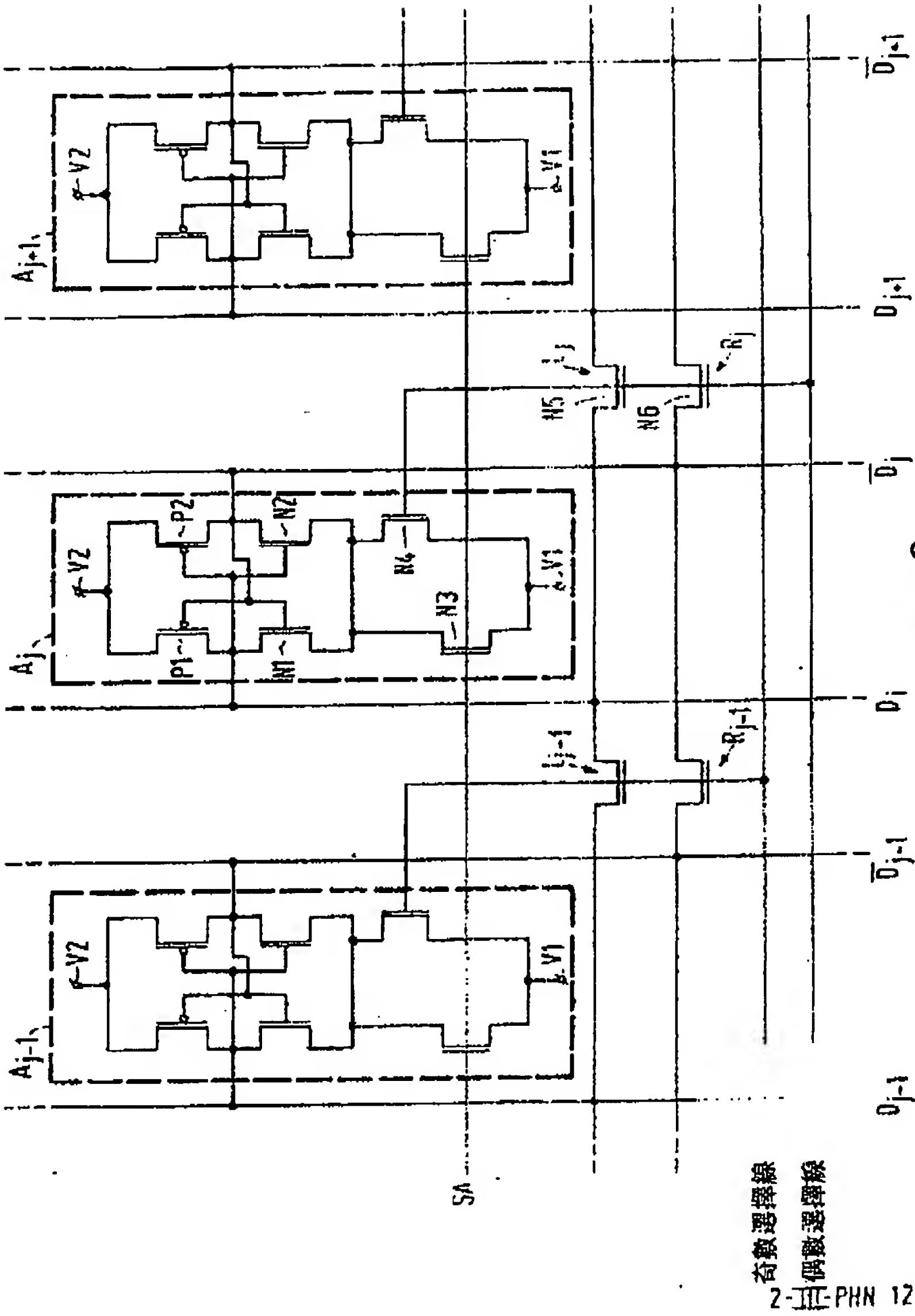

圖 2

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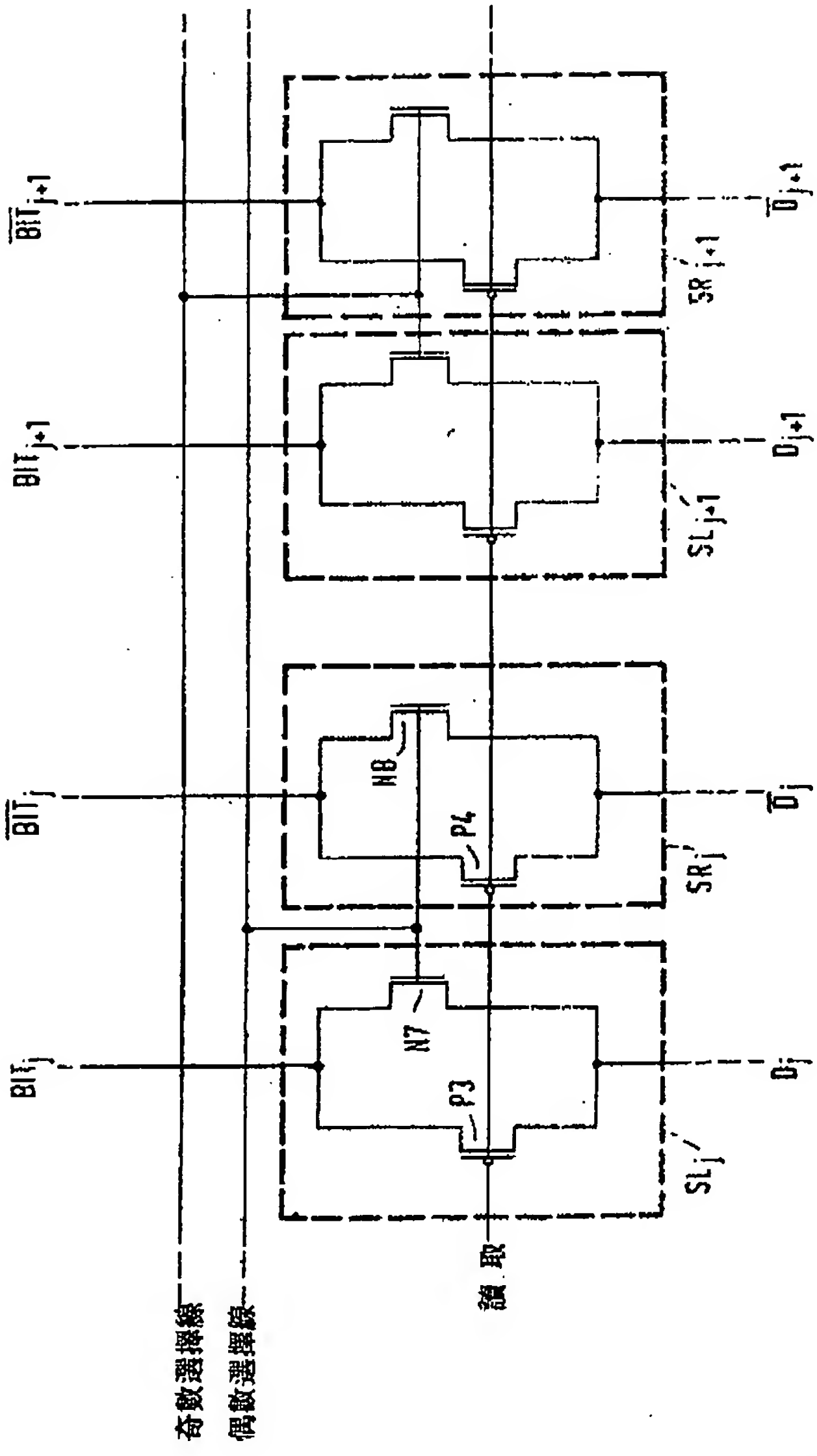

圖 3

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ABSTRACT:

Integrated memory circuit comprising a parallel and serial input and output.

An integrated memory circuit in which memory cells are arranged in rows and columns, each column comprising a separate sense amplifier. Via additional transistors the memory columns can be coupled to neighbouring memory columns and the gain of the sense amplifiers in the even and the odd columns is adjustable. Consequently, information can also be serially shifted from one column to another, so that the information can be written and read not only in parallel but also serially.

Integrated memory circuit comprising a parallel and serial input and output.

The invention relates to an integrated memory circuit, comprising a matrix in which each column comprises its own sense amplifier circuit for forming an externally presentable output signal on a respective sense amplifier circuit output.

A circuit of the kind set forth is known from United States Patent Specification 3,930,239.

Said patent specification describes an integrated memory circuit in which the use of an additional shift register enables fast serial writing and reading of data in the memory. Such a memory circuit has the drawback that a large chip surface area is required for the additional on-chip shift register.

It is inter alia an object of the invention to provide an integrated memory circuit in which data can be quickly written or read, serially or in parallel at option, in or from the memory, but which does not require an additional shift register, allowing the chip surface area of the integrated memory circuit to remain small.

To achieve this, an integrated memory circuit in accordance with the invention is characterized in that each sense amplifier circuit has a latch function, and that there are provided selection means for selecting a number of sense amplifier circuits, each of which forms part of a respective pair of sense amplifier circuits, there also being provided transfer means for directly replacing information of one sense amplifier circuit within the relevant pair by information of the other sense amplifier circuit within the relevant pair, the information of said one sense amplifier circuit thus being destroyed. Said transfer means enable information to or from a memory cell to be applied directly to or transferred directly from an adjacent column. Information can be transported from one column to another so that the information is available in any desired column. Moreover, information can at option be written in or read from the memory in parallel. The memory of the integrated circuit can then be programmed serially, via only one input terminal connected to the chip, by way of

externally supplied data. Subsequently, for example an on-chip microprocessor of the integrated circuit can read the data (for example, instructions which may consist of several bits) from the memory in parallel.

An integrated memory circuit in accordance with the invention offers the advantage that the sense amplifier circuits and the additional switching elements required can be used as a shift register, so that the sense amplifiers have a dual function. The additional switching elements need substantially less chip surface area than the shift register used in the cited reference, so that the total surface area of the integrated memory circuit is smaller.

An embodiment of an integrated memory circuit in accordance with the invention is characterized in that, the one and the other sense amplifier circuit within the pair are directly adjacent, the gain of the one sense amplifier circuit being higher than or equal to the gain of the other sense amplifier circuit under the influence of a control signal. The direction of information transfer from an n^{th} column to an $(n+1)^{th}$ column, or vice versa from the $(n+1)^{th}$ column to the n^{th} column, depends on the respective gains of the sense amplifier circuits in the relevant columns. The information transfer takes place from the column in which the sense amplifier circuit has a higher gain to the column in which the sense amplifier circuit has a lower gain, so that the direction of information transfer is defined. Because the sense amplifier circuits within a pair are directly adjacent, only little chip surface area will be required for the connections between the sense amplifier circuits.

A preferred embodiment of an integrated memory circuit in accordance with the invention is characterized in that the sense amplifier circuits comprise combined inputs and outputs. As a result, a typical flip-flop figuration is obtained where a flip-flop in a column has a master function and a flip-flop in a neighbouring column has a slave function. Without using additional switching means, it is thus possible to write information serially into the memory cells in addition to the serial reading of information from the memory cells.

The invention also relates to an integrated circuit, comprising a processor, a data bus and a memory circuit, the processor being connected, via the data bus, to parallel inputs and outputs of the

memory circuit in accordance with the invention. Thus, any programming of the processor (having, for example an instruction word width of 32 bits) requires only a single connection pin of the integrated circuit (contrary to the 32 connection pins required for parallel programming), resulting in a compact casing for the integrated circuit.

The invention will be described in detail hereinafter with reference to the drawing; therein:

Fig. 1 shows a memory circuit in accordance with the invention,

Fig. 2 is a detailed representation of a preferred embodiment of a part of the memory circuit shown in Fig. 1, and

Fig. 3 is a detailed representation of a preferred embodiment of another part of the memory circuit shown in Fig. 1.

Fig. 1 shows a part of a memory circuit in accordance with the invention. The memory circuit comprises:

- a matrix of memory cells $M_{i,j}$ which are arranged in m rows and n columns, m and n being the number of rows and the number of columns, respectively, which memory cells $M_{i,j}$ in a column j (in this example j is even) are interconnected via two bit lines (BIT_j and $\overline{BIT}_j$), all memory cells in the same row i receiving a row selection signal WL_i,
- in each column j a sense amplifier circuit A_j comprising combined inputs and outputs, all sense amplifier circuits A_j receiving a common control signal via an amplifier control line SA, the sense amplifier circuits in the odd columns and the even columns also receiving a control signal via a first selection line FODD and a second selection line FEVEN, respectively,
- for each column j switchable cascode elements SL_j and SR_j, respectively, which couple the combined inputs and outputs of the sense amplifier circuit A_j, being connected to a data line D_j and $\overline{D}_j$, respectively, in a column j to the bit line BIT_j and $\overline{BIT}_j$, respectively, which elements SL_j and SR_j are connected in all columns j to a common read control line $\overline{READ}$ and, in the odd (1, ..., j-1, j+1, ...) and even (2, ..., j, j+2, ...) columns, are also connected to a first write line WRODD and a second write line WREVEN, respectively,
- switching elements L and R which are capable of connecting, for two

neighbouring columsn j and j+1, the data line D_j to D_{j+1} and $\overline{D}_j$ to $\overline{D}_{j+1}$, the elements L_j and R_j connecting the column j to the adjacent column j+1 by supplying a control signal on the second selection line FEVEN, elements L_{j-1} and R_{j-1} connecting an odd column j-1 to an even column j by way of a control signal on the first selection line FODD.

Hereinafter, signals which must be logic low or logic high will be referred to as "low" and "high", respectively.

The operation of the part of the memory circuit shown in Fig. 1 will be described successively for the reading of information from and the writing of information into the memory cells $M_{i,j}$.

In order to read information from a row of memory cells $M_{i,j}$, the following control signals assume the following logic levels: the control signal on the word line WL_i becomes "high" so that all memory cells $M_{i,j}$ in the row i are selected. As a result, logic signals appear on all bit lines BIT and $\overline{\text{BIT}}$. The control signal on the read control line $\overline{\text{READ}}$ subsequently becomes "low", so that the cascode elements SL_{j-1}, SR_{j-1}, SL_j, SR_j, SL_{j+1}, SR_{j+1} etc. in all columns 1, 2, ..., j, ..., n connect the bit lines BIT_j and $\overline{BIT}_j$ to the sense amplifier circuit A_j and the data lines D_j and $\overline{D}_j$, respectively. When subsequently a "high" control signal appears on the amplifier control line SA, each sense amplifier circuit A_j takes over the information presented on the bit lines BIT_j and $\overline{BIT}_j$ and the data lines D_j and $\overline{D}_j$, amplifies these signals and retains them for the time being.

The information available on the outputs of each sense amplifier circuit A_j and the data lines D_j and $\overline{D}_j$ can subsequently be transferred in parallel to other circuits which are not shown in the drawing, for example to an on-chip micro-processor.

However, it is also possible to transfer the information present on the outputs of each sense amplifier circuit A_j after the reading of a row i of memory cells $M_{i,j}$ serially instead of in parallel to circuits (not shown) in the integrated memory circuit, for example a micro-processor. The serial presentation of information in accordance with the invention is realised as\follows: the data lines D_j and $\overline{D}_j$ in a column j are connected, via switching elements L_j and R_j, to the

data lines D_{j+1} and $\bar{D}_{j+1}$ in a directly adjacent column j+1. The drawing shows that switching elements L_{j-1} and R_{j-1} connect the data lines D_{j-1} and $\bar{D}_{j-1}$, respectively, in the column j-1 to the data lines D_j and $\bar{D}_j$, respectively, in the column j, and that switching elements L_j and R_j connect the data lines D_j and $\bar{D}_j$, respectively, in the column j to the data lines D_{j+1} and $\bar{D}_{j+1}$, respectively, in the column j+1. When the switching elements L_{j-1} and R_{j-1}, L_{j+1} and R_{j+1} etc. are selected by a "high" selection signal on the line FODD, while the switching elements L_j and R_j, L_{j+2} and R_{j+2} (not shown in the drawing) etc. are not selected because of a "low" signal on the line FEVEN, information can flow from the column j-1 to the column j or vice versa from the column j to the column j-1. Similarly, information can flow from the column j+1 to the column j+2 or vice versa from the column j+2 to the column j+1, etc. The direction of information transfer, from a column j to a column j+1 or vice versa from a column j to a column j-1, depends on the gains of the sense amplifier circuits A_{j-1}, A_j, A_{j+1}, A_{j+2} in the relevant columns j-1, j, j+1, j+2. The control signal on the amplifier control line SA is "high" during the serial transfer, so that a sense amplifier circuit receiving information from a neighbouring sense amplifier circuit can take over and retain this information. The information transfer takes place from a column with a sense amplifier circuit of higher gain to a column comprising a sense amplifier circuit of lower gain, the information in the latter column being lost because the information originally present therein is replaced by new information from the adjacent column in which the gain of the sense amplifier circuit is higher.

The required discrimination between the gains of the sense amplifier circuits is also realised by means of the signals on the selection lines FODD and FEVEN. In the presence of a selection signal on the line FODD and absence of a selection signal on the line FEVEN, the gain of, for example the sense amplifier circuit A_{j-1} is higher than the gain of the sense amplifier circuit A_j. Because in Fig. 1 the sense amplifier circuits A_{j-1}, A_{j+1}, etc. and the switching elements L_{j-1} and R_{j-1}, L_{j+1} and R_{j+1}, etc. all receive a control signal via the line FODD, and the sense amplifier circuits A_j, A_{j+2} etc. and the switching elements L_j and R_j, L_{j+2} and R_{j+2} etc. all

receive a control signal via the line FEVEN, the information transfer takes place from the column j to a column j+1. When the drive of the sense amplifier circuits A_j and A_{j-1} is reversed (replacing each drive via the lines FODD and FEVEN by a drive via the line FEVEN and FODD, respectively) and the drive for the switching elements L_j and R_j remains the same, or when the drive of the switching elements L_j, R_j and L_{j-1}, R_{j-1} is reversed and the drive of the sense amplifier circuits A_j remains the same, the latter direction of information transfer is reversed and information is transferred from a column j to a column j-1. However, addition of simple multiplex circuits and a control signal to be applied thereto enable the information transfer to take place as desired from the column j to the column j+1 or from the column j to the column j-1. The additional control signal makes the multiplexer circuits connect the sense amplifier circuits A_j, A_{j+2} etc. to either the line FODD or the line FEVEN, and the sense amplifier circuits A_{j-1} and A_{j+1} to either the line FEVEN or the line FODD. In the former case, the information transfer takes place from right to left and in the second case from left to right. For the sake of simplicity, hereinafter a signal on a line will be denoted by the symbol of the relevant line.

For serial transfer of information to circuits (not shown) in the integrated memory circuit, control signals FODD and FEVEN assume the following levels, viewed in time: control signal SA is "high", control signal FODD is "high" and control signal FEVEN is "low", so that information transfer takes place from the column j-1 to the column j, from the column j+1 to the column j+2 etc. Subsequently, the control signal FODD becomes "low" and the control signal FEVEN becomes "high", so that information transfer takes place from the column j to the column j+1, from the column j+2 to the column j+3 etc. The control signal FODD becomes "high" again and the control signal FEVEN becomes "low" again, so that a data transfer takes place to a next column, etc. The control signals FODD and FEVEN alternately become "high" and "low" until all desired information has been transferred to circuits (not shown) in the integrated memory circuit. The described sequence of control signals FODD and FEVEN ensures the presentation of the memory information in the odd columns j-1, j+1, etc., via the last column n in the memory circuit, to circuits (not shown) in the integrated memory circuit. Using a

sequence of control signals FODD and FEVEN which is similar to the one described above, be it with an initial value of FODD and FEVEN which, after the memory information has become available on all combined inputs and outputs of the sense amplifier circuits A_j, is "low" and "high", respectively, the information is presented from the even columns j, j+2, etc. to circuits (not shown) in the integrated memory circuits. The serial reading of a full row of memory cells $M_{i,j}$ should, therefore, take place in two steps, i.e. serial reading of the odd columns j-1, j+1 etc., followed by the reading of the even columns j, j+2 etc., or the reading of the even columns, followed by the odd columns of the memory circuit.

The writing of information in a row i of memory cells $M_{i,j}$ can also be realised in two different ways as already described for the reading of information from the memory cells, i.e. in parallel or serially. In the case of parallel presentation of information on the data lines D_j and $\overline{D}_j$, this information is taken over and retained in the presence of a "high" control signal SA. Subsequently, in the presence of "high" signals WRODD, WREVEN and WL_i this information is stored in the memory cells $M_{i,j}$ in the row i. Alternatively, information can be stored in the memory cells $M_{i,j}$ by means of other drivers (not shown in Fig. 1) coupled to the data lines D_{j-1} and $\overline{D}_{j-1}$, D_j and $\overline{D}_j$, D_{j+1} and $\overline{D}_{j+1}$ etc. instead of by means of sense amplifier circuits A_{j-1}, A_j, A_{j+1} etc. In the present example the serial writing of information in a row of memory cells is performed as follows: information is presented to the data lines D_1 and $\overline{D}_1$ of the first column 1 in the memory circuit. The control signal SA is "high". Subsequently, the control signal FODD becomes "high" and the control signal FEVEN remains "low". Consequently, the sense amplifier circuit A_2 in the adjacent second column 2 takes over this information. Subsequently, the control signal FEVEN becomes "high" and FODD becomes "low", so that this information is taken over by the sense amplifier circuit A_3 in the third column 3. Subsequently, new information is presented to the data lines D_1 and $\overline{D}_1$ of the first memory column 1, after which the control signal FODD becomes "high" and FEVEN becomes "low" again etc. Thus, information is serially shifted from the column j to the column j+1. Like in the preceding description of the serial reading of memory cells, the serial writing of

information in a row of memory cells must also take place in two steps. During the first step, writing takes place, for example in the i^{th} row in the memory cells in the odd columns and in a second step in the memory cells in the even columns or vice versa. Using the control signals WRODD and WREVEN, driving the cascode elements SL and SR, the information shifted to the sense amplifier circuits during the first and the second step, respectively, can be written in the memory cells of the odd and the even columns, respectively, or of the even and the odd columns, respectively.

Fig. 2 is a detailed representation of a preferred embodiment of a part of the memory circuit shown in Fig. 1, that is to say a preferred embodiment of the switching elements L_{j-1} and R_{j-1}, L_j and R_j etc. and the sense amplifier circuits A_{j-1}, A_j, A_{j+1} etc. The switching elements L_{j-1} and R_{j-1}, L_j and R_j etc. each comprise an n-type transistor N5 and N6 and each sense amplifier circuit A comprises four n-type transistors N1, N2, N3 and N4, and two p-type transistors P1 and P2. The sources of the transistors N1 and N2 are connected to one another and to the drains of the transistors N3 and N4. The drains of the transistors N1 and P1 and of the transistors N2 and P2 are connected to one another, to the gates of the transistors N2 and P2 and N1 and P1, respectively, and to the data line D and $\overline{D}$, respectively. The sources of the transistors P1 and P2 and of the transistors N3 and N4 are coupled to power supply terminals V2 and V1, respectively. The gate of the transistor N3 and of the transistor N4 in the column j receives a control signal SA and a control signal FEVEN, respectively.

The circuit shown in Fig. 2 operates as follows: in the case of a "high" control signal FEVEN, a "low" control signal FODD and a "high" control signal SA, the transistors N3 and N4 are both turned on and a comparatively large current flows to the first power supply terminal V1. Consequently, the gain of the sense amplifier circuit A_j exceeds that of the sense amplifier circuit A_{j+1} which is driven only by the control signal SA and not by the control signal FODD so that, as has already been mentioned in the description of the operation of the circuit shown in Fig. 1, information is transferred from the column j to the neighbouring column j+1.

Fig. 3 is a detailed representation of a preferred

embodiment of the cascode elements SL_j and SR_j, SL_{j+1} and SR_{j+1} etc. shown in Fig. 1. Each of the cascode elements SL and SR comprises a parallel connection of an n-type transistor N7 and N8, respectively, and a p-type transistor P3 and P4, respectively. The gates of the transistors N7 and N8 in the even (2, 4, 6, ...) memory columns and the odd (1, 3, 5, ...) memory columns are coupled to control signals WREVEN and WRODD, respectively. The gates of the transistors P3 and P4 in the cascode elements SL and SR in each memory column are controlled by the control signal $\overline{READ}$.

The circuit shown in Fig. 3 operates as follows: the functions of the cascode elements SL and SR have already been described with reference to Fig. 1, so that only the functions of the n-type and p-type transistors will be elucidated. In the case of a "low" control signal $\overline{READ}$, the transistors P3 and P4 in all cascode elements SL and SR in the memory circuit are turned on, so that in each column j the bit line BIT_j is connected to the data line D_j and the bit line $\overline{BIT}_j$ is connected to the data line $\overline{D}_j$. The use of p-type transistors instead of n-type transistors for the transistors P3 and P4 is to be preferred, because the voltages on the bit lines BIT_j and $\overline{BIT}_j$ are usually greater than the sum of the control voltage $\overline{READ}$ plus the threshold voltage V_{THP} of a p-type transistor when information is read from a memory cell $M_{i,j}$ (this sum is approximately equal to 1 V in the case of a supply voltage of, for example 5 V), so that no voltage loss occurs across the transistors P3 and P4. For the transistors N7 and N8 preferably n-type transistors are used, because the transistors which connect the memory cells $M_{i,j}$ to the bit lines BIT_j and $\overline{BIT}_j$ (not shown in the Figure) are usually also n-type transistors, so that in the case of a write operation in the memory cells $M_{i,j}$ via the bit lines BIT_j and $\overline{BIT}_j$ no threshold voltage loss occurs for a "low" level.

第78110052號專利申請案
英文申請專利範圍修正本(79年3月)

Chinese Patent Application No. 78110052
Amended Claims (March 1990)

1. An integrated memory circuit, comprising a matrix in which each column comprises its own sense amplifier circuit for forming an externally presentable output signal on a respective sense amplifier circuit output, characterized in that each sense amplifier circuit has a latch function and that there are provided selection means for selecting a number of sense amplifier circuits, each of which forms part of a respective pair of sense amplifier circuits, there also being provided transfer means for directly replacing information of one sense amplifier circuit within the relevant pair by information of the other sense amplifier circuit within the relevant pair, the information of said one sense amplifier circuit thus being destroyed.

2. An integrated memory circuit as claimed in Claim 1, wherein, the one and the other sense amplifier circuit within the pair are directly adjacent, the gain of the one sense amplifier circuit being higher than or equal to the gain of the other sense amplifier circuit under the influence of a control signal.

3. An integrated memory circuit as claimed in Claim 2, wherein the sense amplifier circuits comprise combined inputs and outputs.

4. An integrated memory circuit as claimed in Claim 3, wherein each input of a sense amplifier circuit in a column is connected to a bit line in the relevant column via a separately switchable cascode element which is suitable for the reception of two different control signals.

5. An integrated memory circuit as claimed in Claim 3, wherein each switchable series element comprises an n-type transistor.

6. An integrated memory circuit as claimed in Claim 4, wherein each switchable cascode element comprises a parallel connection of a p-type transistor and an n-type transistor.

7. An integrated memory circuit as claimed in Claim 5, wherein control electrodes of the n-type transistors, from

an odd to an even column bearing an increasing column number, are suitable for the reception of a first control signal and, from an even to an odd column bearing an increasing column number, suitable for the reception of a second control signal.

8. An integrated memory circuit as claimed in Claim 6, wherein the control electrode of the p-type transistor in each switchable cascode element is suitable for the reception of a read signal, the control electrode of the n-type transistor in each switchable cascode element in an odd and an even column being suitable for the reception of a first and a second write signal, respectively.

9. An integrated memory circuit as claimed in Claim 7, wherein the sense amplifier circuit in an odd and an even column is suitable for the reception of the first and the second control signal, respectively, or the second and the first control signal, respectively.

10. An integrated memory circuit as claimed in Claim 9, in which each sense amplifier circuit can be switched on or off by means of an n-type transistor, wherein parallel to the latter n-type transistor there is connected an additional n-type transistor whose control electrode is suitable for the reception of the first or the second control signal.

11. An integrated memory circuit as claimed in Claim 5, 6, 7, 8 or 10, wherein an n-type transistor is either an n-channel field effect transistor or a bipolar npn transistor, a p-type transistor being either a p-channel field effect transistor or a bipolar pnp transistor.

12. An integrated circuit, comprising a processor, a data bus and a memory circuit, the processor being connected, via the data bus, to parallel inputs and outputs of the memory circuit as claimed in Claim 1.

13. An integrated circuit as claimed in Claim 12, wherein a serial input/output of the memory circuit is connected to a connection pin of the integrated circuit.

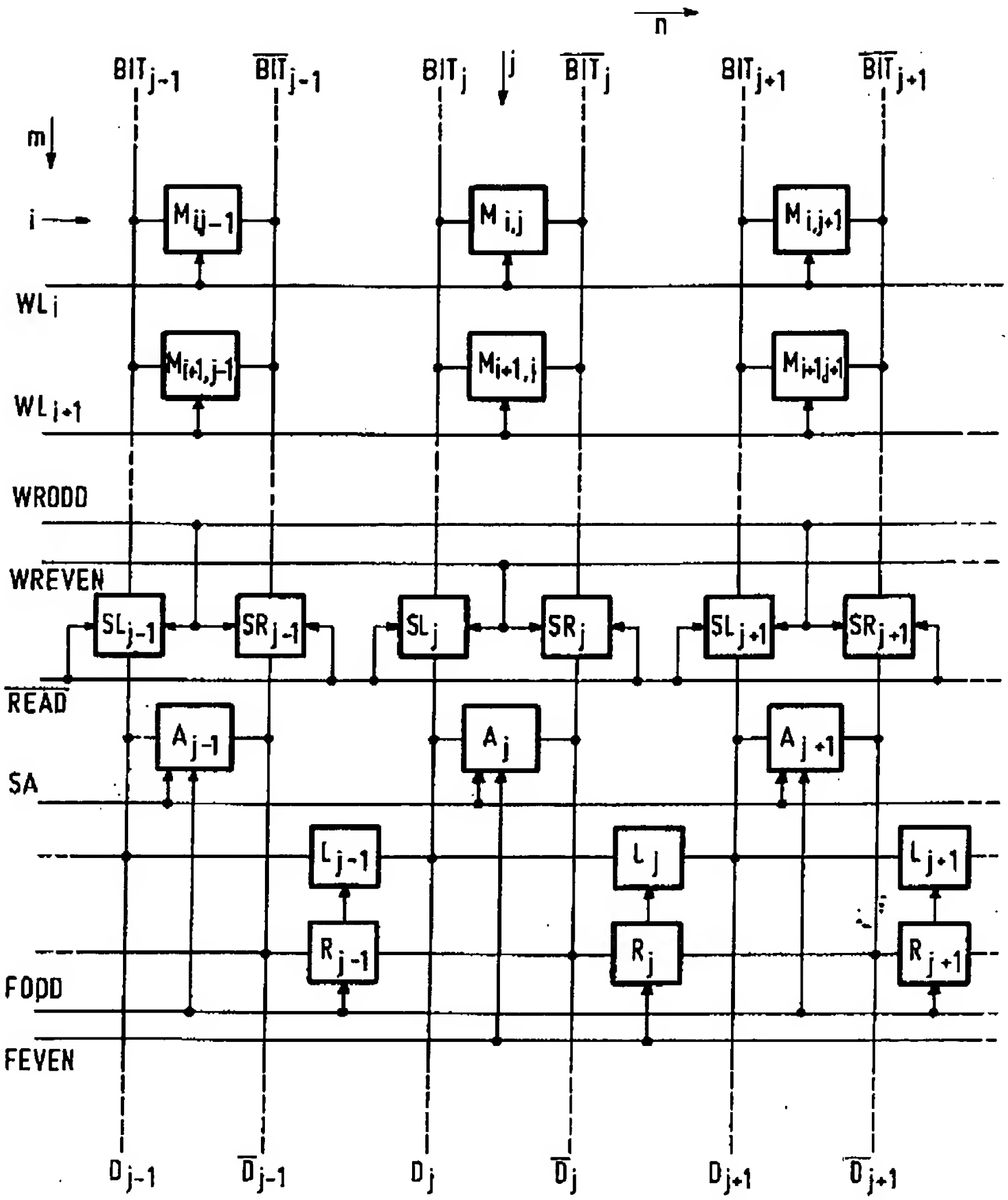

FIG. 1

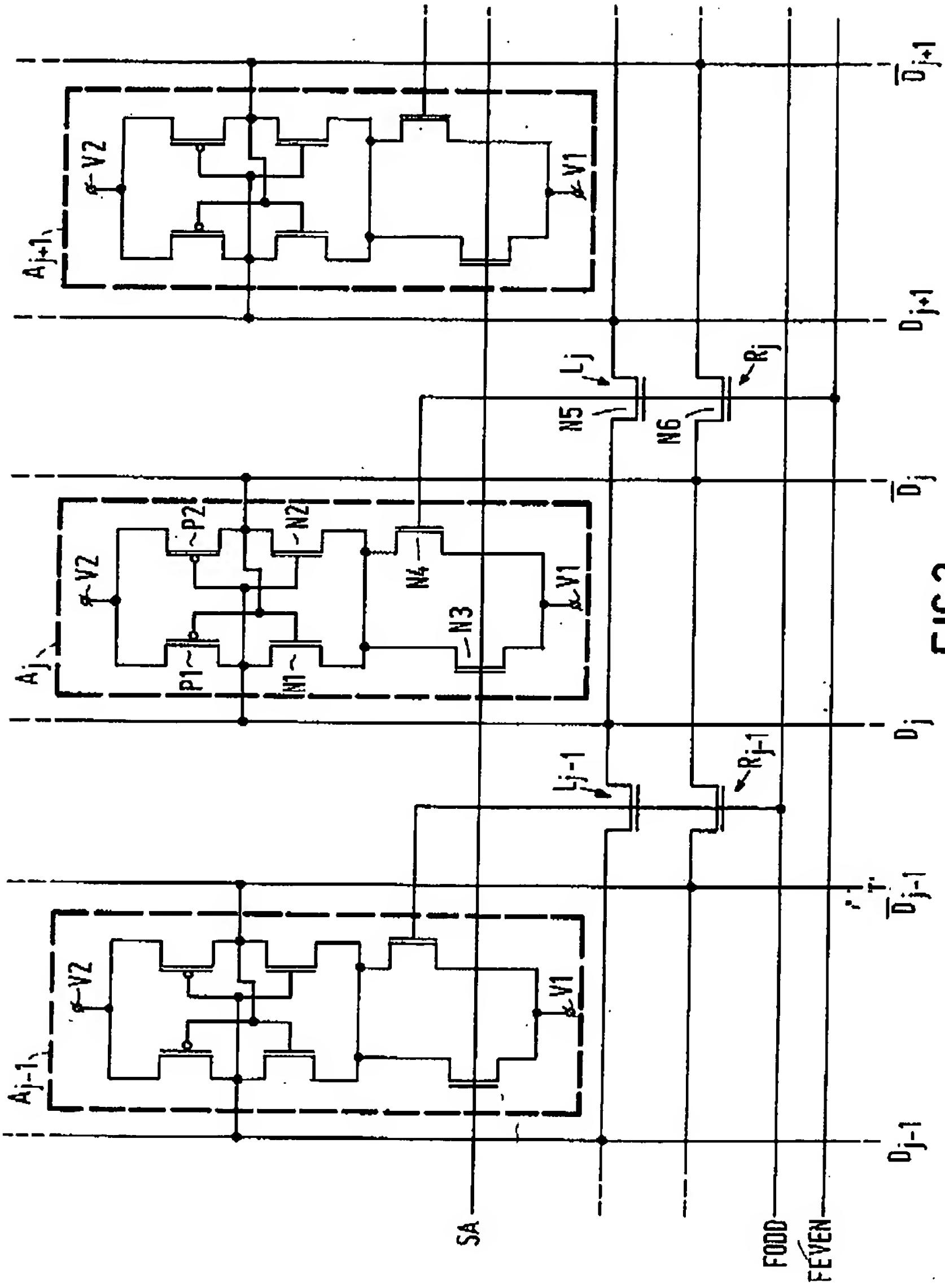
V2
V1
A_{j+1}
$\overline{D_{j+1}}$
D_{j+1}
L_j
R_j
N5
N6
$\overline{D_j}$
P2
N2
N4
N3
P1
N1
A_j
D_j
L_{j-1}
R_{j-1}
A_{j-1}
$\overline{D_{j-1}}$
D_{j-1}
SA
FODD
FEVEN

FIG.2

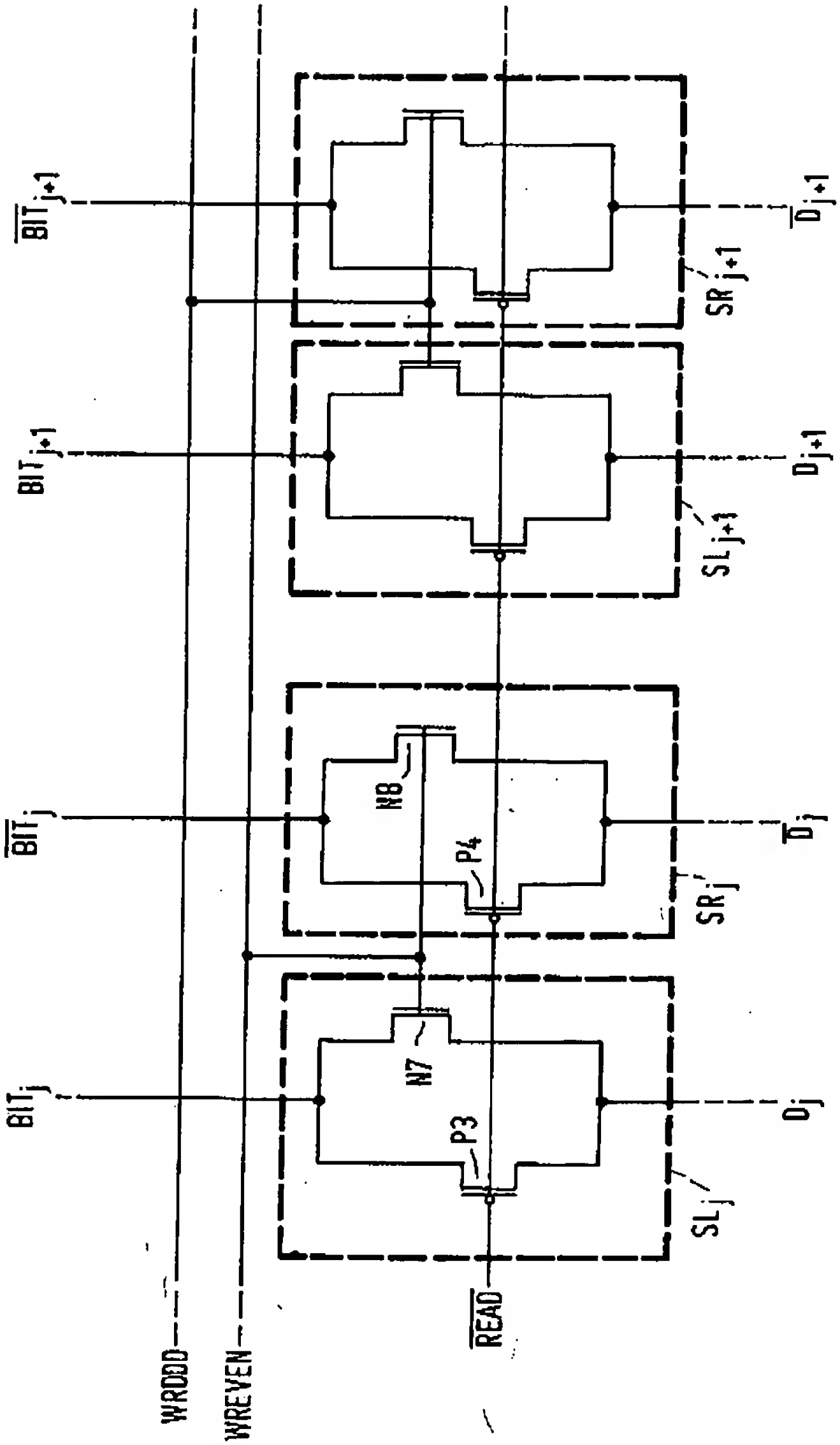

FIG.3